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PRE-APPEAL BRIEF REQUEST FOR REVIEW		Docket Number (Optional) YOR920030603US1
I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to "Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450" [37 CFR 1.8(a)] on _____ Signature _____ Typed or printed name _____	Application Number 10/751,714	Filed January 5, 2004
First Named Inventor Luk et al.		
Art Unit 3663		
Examiner J.P. Mondt		
<p>Applicant requests review of the final rejection in the above-identified application. No amendments are being filed with this request.</p> <p>This request is being filed with a notice of appeal.</p> <p>The review is requested for the reason(s) stated on the attached sheet(s). Note: No more than five (5) pages may be provided.</p>		
I am the <input type="checkbox"/> applicant/inventor. <input type="checkbox"/> assignee of record of the entire interest. See 37 CFR 3.71. Statement under 37 CFR 3.73(b) is enclosed. (Form PTO/SB/96) <input type="checkbox"/> attorney or agent of record. Registration number _____ <input checked="" type="checkbox"/> attorney or agent acting under 37 CFR 1.34. Registration number if acting under 37 CFR 1.34 39,411	<div style="text-align: center;">  _____ Signature Paul J. Otterstedt _____ Typed or printed name 203-255-6560 _____ Telephone number October 22, 2008 _____ Date </div>	
NOTE: Signatures of all the inventors or assignees of record of the entire interest or their representative(s) are required. Submit multiple forms if more than one signature is required, see below".		
<input type="checkbox"/> *Total of _____ forms are submitted.		

This collection of information is required by 35 U.S.C. 132. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.11, 1.14 and 41.6. This collection is estimated to take 12 minutes to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Mail Stop AF, Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent Application

5 Applicant(s): Luk et al.
Docket No: YOR920030603US1
Serial No.: 10/751,714
Filing Date: January 5, 2004
Group: 3663
10 Examiner: J. P. Mondt

Title: Amplifiers Using Gated Diodes

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MEMORANDUM IN SUPPORT OF
PRE-APPEAL BRIEF REQUEST FOR REVIEW

20 Mail Stop AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

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Sir:

The present invention and prior art have been summarized in Applicants' prior
30 responses.

REMARKS

The present application was filed on January 5, 2004 with claims 1 through 42. Claims 38-42 were cancelled in the Amendment and Response to Office Action dated December 13, 2005. Claims 21-23 and 29-35 were withdrawn due to a restriction requirement. Claims 1-20 were cancelled in the Amendment and Response to Office Action dated January 29, 2008. Claims 21-23 and 29-35 were cancelled in the Amendment and Response to Office Action dated May 6, 2008. Claims 24-28, 36 and 37 are presently pending in the above-identified patent application.

In the Office Action, the Examiner rejected claims 24-28, 36 and 37 under 35 U.S.C. 102(b) as being anticipated by Folmsbee (United States Patent No. 5,386,151).

Independent Claim 24

Independent claim 24 was rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee. In particular, the Examiner asserts that Folmsbee discloses determining that a voltage on a signal line (signal line from VDD to node 125) is to be amplified; and modifying voltage on a control line ϕ' (providing clock input ϕ' under gate of MOS capacitor 130) (col. 4, lines 1-33), wherein the control line is coupled to a second terminal (source-drain terminal) of a two terminal semiconductor device (MOS capacitor 130). In the Response to Arguments section of the final Office Action, the Examiner asserts that this argument is not persuasive because, even by admission (FIG. 2 and discussion of the present specification), a gated diode is a two-terminal device while having source, gate and drain, with source and drain short-circuited. The Examiner asserts that this terminology is standard in the field of MOS capacitors and MOSFETs.

Applicants note that the Examiner equates the signal line of claim 24 with the line from VDD to node 125. Applicants note that a *signal line carries information*, as would be apparent to a person of ordinary skill in the art. The IEEE Standard Dictionary of Electrical and Electronic Terms defines a signal as, *for example*, "...carrying binary true/ false logic values." The line from VDD to node 125 does not carry information.

In the Response to Arguments section of the final Office Action, the Examiner asserts that "no example can possibly be a definition."

First, Applicants note it was argued that a signal line is defined as a line that "carries information"; this is a definition and *not* an example. Second, the IEEE Standard

Dictionary of Electrical and Electronic Terms definition was provided in support of this definition. Finally, contrary to the Examiner's assertion, many terms have more than one definition, as would be apparent to a person of ordinary skill in the art. Applicants used the phrase "for example" to acknowledge that different sources often provide different definitions of a term.

In the Response to Arguments section of the final Office Action, the Examiner asserts that "the variable voltage VDD not only can be used, and actually is used, in the method employing the device by Folmsbee, to convey information on control, because the voltage source VDD is a modified signal carrying information upon arrival at node 125."

Applicants note that Folmsbee teaches that VDD is "a supply voltage." (Col. 4, line 16.) Contrary to the Examiner's assertion, a "supply voltage" is *not a signal*, in accordance with the well known definition of the term and, furthermore, Folmsbee does *not* disclose or suggest that VDD is a signal or that VDD conveys information.

In addition, MOS capacitor 130 is a three terminal device (gate, source, and drain), as would be apparent to a person of ordinary skill in the art. The connection of the source terminal to the drain terminal does *not* reduce the terminal count of the device.

Thus, Folmsbee does not disclose or suggest determining that a voltage on a signal line is to be amplified and does not disclose or suggest wherein the control line is coupled to a second terminal of a two terminal semiconductor device, as required by independent claim 24.

Dependent Claims 25-28, 36 and 37

Dependent claims 25-28, 36, and 37 were rejected under 35 U.S.C. 102(b) as being anticipated by Folmsbee.

Claims 25-28, 36, and 37 are dependent on claim 24 and are therefore patentably distinguished over Folmsbee because of their dependency from independent claim 24 for the reasons set forth above, as well as other elements these claims add in combination to their base claim.

Since all of the pending claims, i.e., claims 24-28, 36 and 37, are in condition for allowance, such favorable action is earnestly solicited.

If any outstanding issues remain, or if the Examiner has any further suggestions for expediting allowance of this application, the Examiner is invited to contact the undersigned at the telephone number indicated below.

The Examiner's attention to this matter is greatly appreciated.

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Respectfully submitted,



Date: October 22, 2008

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